AMENDMENTS TO THE CLAIMS

Upon entry of the present amendment, the status of the claims will be as shown below. This listing of claims replaces all previous versions and listings of the claims in the present application.

Listing of Claims:

1 (Currently Amended). A display, comprising:

a plurality of discharge cells;

a clock signal generator that generates a clock signal;

a serial data generator that generates serial data according to an image to be displayed;

a test signal generator that generates a test signal;

a data driver that selectively applies a drive pulse to said plurality of discharge cells based on the serial data generated by said serial data generator in synchronization with said clock signal in a write period for selecting a discharge cell to be lighted;

a latch failure detector that includes a lather that latches the test signal generated by said test signal generator to detect a ~~detects the~~ presence/absence of a latch failure in said data driver based on an output signal from said lather ~~the test signal generated by the test signal generator~~ in a period other than said write period; and

a phase adjuster that, when the latch failure is detected by said latch failure detector, adjusts a phase of the clock signal provided from said clock signal generator to said data driver, based on the phase of the clock signal in which the latch failure is detected [[,]] .

~~wherein the phase adjustment of the clock signal is only made if a phase of the serial data and the phase of the clock signal differ at least a predetermined amount such that a latch failure is detected.~~

2 (currently amended). The display according to claim 1,

wherein said data driver includes a plurality of data drivers;

said latch failure detector includes a plurality of latch failure ~~detecting circuits~~ detectors that detect the presence/absence of the latch failure by [[the]] respective data drivers based on the test signal outputted from said test signal generator; and

when the latch failure is detected in at least one of said plurality of latch failure ~~detecting circuits~~ detectors, said phase adjuster adjusts the phase of the clock signal provided to said plurality of data drivers from said clock signal generator.

3 (currently amended). The display according to claim 2,

wherein said plurality of latch failure ~~detecting circuits~~ detectors each have an open drain output; and

said phase adjuster receives the open drain outputs of said plurality of latch failure ~~detecting circuits~~ detectors via a wired-OR connection.

4 (previously presented). The display according to claim 1, wherein said test signal is an alternating pulse signal that is inverted every period of said clock signal.

5 (previously presented). The display according to claim 1, wherein said phase adjuster adjusts the phase of the clock signal at predetermined intervals.

6 (previously presented). The display according to claim 1, wherein said phase adjuster adjusts the phase of the clock signal at intervals of a plurality of fields.

7 (previously presented). The display according to claim 1, wherein said phase adjustment includes a plurality of phase adjustment periods; and

said phase adjuster continues, when the adjustment of said phase of the clock signal has not finished in one adjustment period, the phase adjustment of said phase of the clock signal from the beginning of the next adjustment period.

8 (previously presented). The display according to claim 4, wherein said latch failure detector generates a latch failure detection signal indicating the presence/absence of the latch failure, based on an exclusive logical sum of a first test signal obtained by delaying said test signal by one period of said clock signal and a second test signal obtained by delaying said test signal by two periods of said clock signal.

9 (previously presented). The display according to claim 8, wherein said latch failure detector generates a plurality of latch failure detection signals obtained by sequentially delaying said latch failure detection signal by a predetermined delay amount to generate a logical product of said plurality of latch failure detection signals.

10 (currently amended). The display according to claim 1, wherein said latch failure detector includes a ~~holding circuit~~ holder that holds a detection result of the latch failure until a reset signal is inputted.

11 (currently amended). The display according to claim 10, wherein said latch failure detector further includes a reset signal ~~generating circuit~~ generator that generates said reset signal based on the detection result of the latch failure.

12 (canceled).

13 (previously presented). The display according to claim 1,

wherein said phase adjuster includes:

a ring buffer including a plurality of delay elements that sequentially delay said clock signal by a predetermined delay amount; and

a selector that selectively outputs a plurality of clock signals outputted from said plurality of delay elements of said ring buffer.

14 (currently amended). The display according to claim 1,

wherein said phase adjuster includes:

a plurality of ~~delay circuits~~ delays each having a different number of delay amounts; and

a ~~connecting circuit~~ connector that selects one or more of said plurality of ~~delay circuits~~ delays so as to constitute a ~~series-connecting circuit~~ series-connector by the selected one or more of said plurality of ~~delay circuits~~ delays and provides said clock signal to ~~said series-connecting circuit~~ series-connector.

15 (canceled).

16 (previously presented). The display according to claim 1, wherein the phase adjuster is operable to detect that the phase of the adjusted clock signal is an optimal phase and finish the adjustment of the phase of said clock signal when it is detected that the phase of the clock signal is the optimal phase.

17 (previously presented). The display according to claim 1, further comprising a first storage that stores the phase of the clock signal adjusted by said phase adjuster as an optimal phase,

wherein said phase adjuster adjusts the phase of said clock signal to said optimal phase stored in said first storage in a write period after said optimal phase is stored by said first storage.

18 (previously presented). The display according to claim 17, wherein said phase adjuster adjusts the phase of said clock signal to a phase stored in advance in said first storage when the adjustment of said phase of the clock signal has not finished in said adjustment period.

19 (currently amended). The display according to claim 17, wherein said phase adjuster varies the phase of said clock signal to detect a range of phases where no latch failure occurs and when the detected range is larger than a predetermined threshold, stores, in said first storage, a phase in [[the]] a center of said detected range of phases as said optimal phase.

20 (previously presented). The display according to claim 17, wherein said phase adjuster adjusts a relative phase of the clock signal with respect to said serial data so that said adjusted phase of the clock signal is outputted to the data driver just as a phase of a start portion of said serial data is outputted to said data driver.

21 (previously presented). The display according to claim 20, wherein, said phase adjuster adjusts the phase of said serial data so that the phase of the start portion of the serial data outputted to said data driver and a phase of a start portion of the clock signal outputted to said

data driver substantially coincide with each other when it is detected that the phase of said clock signal is the optimal phase.

22 (previously presented). The display according to claim 21, further comprising a second storage that stores the phase of said serial data adjusted by said phase adjuster as an optimal phase,

wherein said phase adjuster adjusts the phase of said serial data to said optimal phase stored in said second storage in the write period after said optimal phase is detected by said second storage.

23 (previously presented). The display according to claim 22, wherein said phase adjuster adjusts the phase of said clock signal to the optimal phase stored in said first storage a last time and adjusts the phase of said serial data to the optimal phase stored in said second storage a last time when the optimal phase of said clock signal or the optimal phase of said serial data is not detected.

24 (previously presented). The display according to claim 1, wherein an adjustment period is set to a sustain period during which light emitting of the discharge cell selected in said write period is sustained.

25 (new). A display, comprising:

a plurality of discharge cells;

a clock signal generator that generates a clock signal;

a serial data generator that generates serial data according to an image to be displayed;

a test signal generator that generates a test signal;

a data driver that selectively applies a drive pulse to said plurality of discharge cells based on the serial data generated by said serial data generator in synchronization with said clock signal in a write period for selecting a discharge cell to be lighted;

a latch failure detector that detects a presence/absence of a latch failure in said data driver in accordance with the test signal generated by said test signal generator in a period other than said write period; and

a phase adjuster that, when the latch failure is detected by said latch failure detector, adjusts a phase of the clock signal provided from said clock signal generator to said data driver, based on the phase of the clock signal in which the latch failure is detected,

wherein the phase adjustment of the clock signal is only made when the latch failure has been detected, said latch failure being detected when a width of a latch failure non-occurrence region is larger than a predetermined threshold.

26 (new). A display, comprising:

a plurality of discharge cells;

a clock signal generator that generates a clock signal;

a serial data generator that generates serial data according to an image to be displayed;

a test signal generator that generates a test signal;

a data driver that selectively applies a drive pulse to said plurality of discharge cells based on the serial data generated by said serial data generator in synchronization with said clock signal in a write period for selecting a discharge cell to be lighted;

a latch failure detector having a lather that latches the test signal generated by said test signal generator to detect a presence/absence of a latch failure in said data driver based on an output signal from said lather in a period other than said write period; and

a phase adjuster that, when the latch failure is detected by said latch failure detector, adjusts a phase of the clock signal provided from said clock signal generator to said data driver, based on the phase of the clock signal in which the latch failure is detected,

wherein the phase adjustment of the clock signal is only made when the latch failure has been detected, said latch failure being detected when a width of a latch failure non-occurrence region is larger than a predetermined threshold